

MS-7037

Version 20A
05/06/2004 Update

Intel (R) Springdale (GMCH) + ICH5 Chipset
Intel Northwood & Prescott mPGA478B Processor

CPU:

Intel Northwood/Prescott - 3.6G & Above

System Chipset:

Intel Springdale - GMCH (North Bridge) 848P
Intel ICH5 (South Bridge)

On Board Chipset:

CLOCK -- Cypress CY28405

On Board Chipset:

BIOS -- FWH EEPROM 4M
AC'97 Codec -- REALTEK / ALC655
LPC Super I/O -- W83627THF
LAN - REALTEK RTL8110S/8100C
1394 - VIA 6307

Main Memory:

DDR * 2

Expansion Slots:

PCI2.3 SLOT * 3
AGP4X/8X SLOT * 1

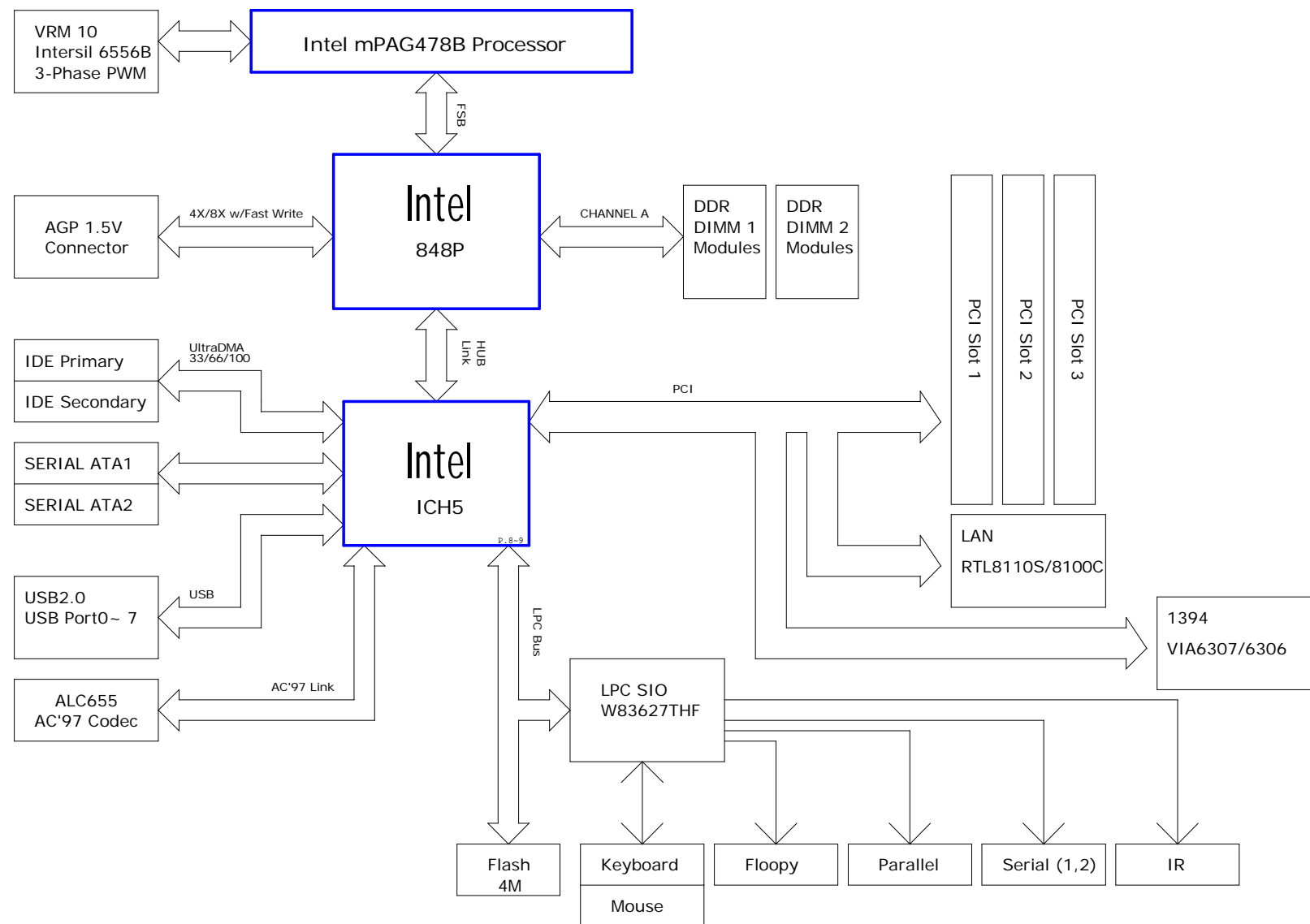
ST PWM:

Controller: INTERSIL 6556B

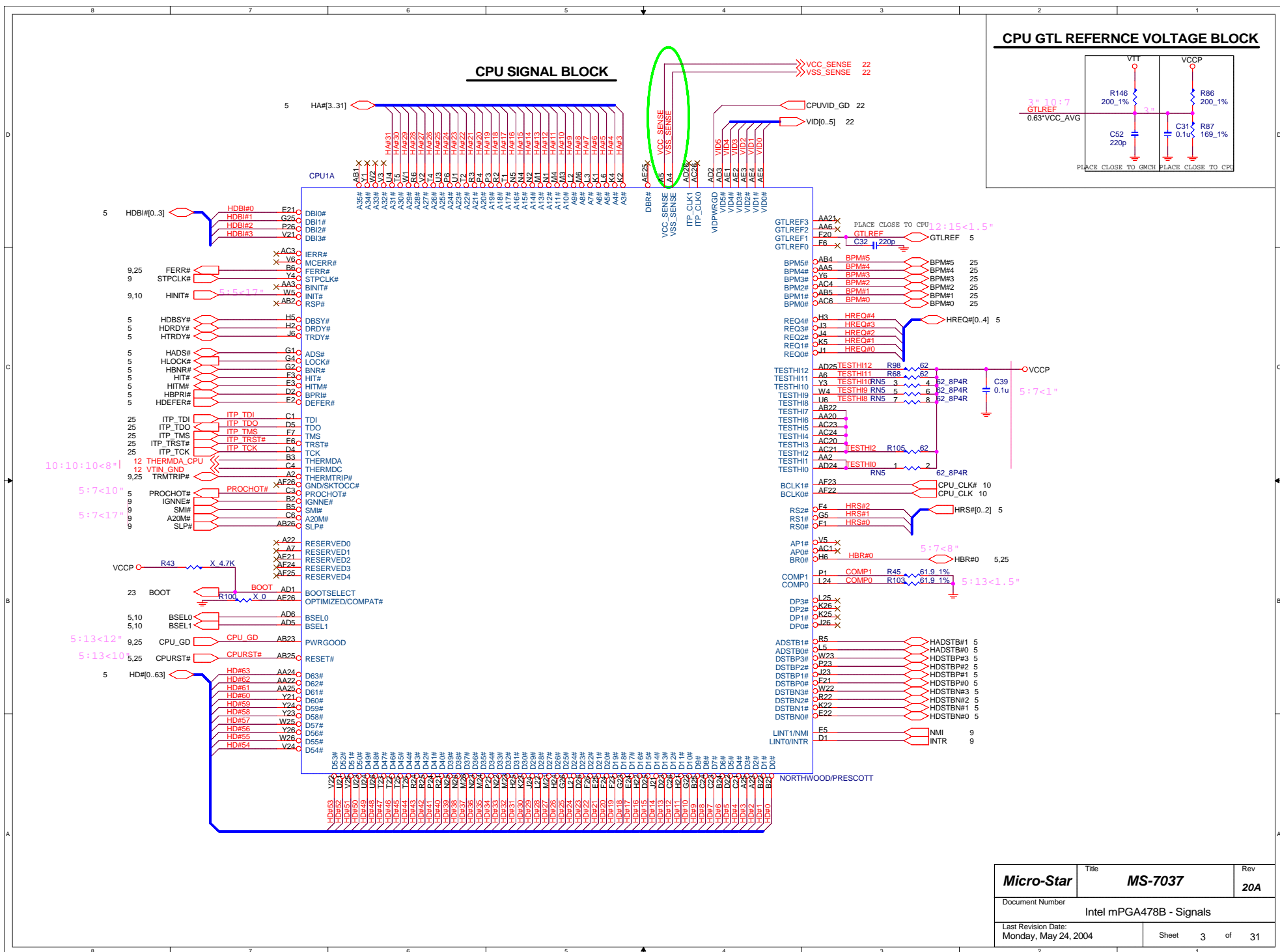
ERP BOM	Function Description	
501/601-7037	Opt : STD	848P+ICH5,W/LAN-8100,W/655,W/1394-6307
06S---		
501/601-7037	Opt : I	848P+ICH5,WO/LAN-8100,W/655,W/1394-6307
07S---		

Title	Page
Cover Sheet	1
Block diagram	2
Intel µPGA478B CPU - Signals	3
Intel µPGA478B CPU - Power	4
Intel Springdale - Host Signals	5
Intel Springdale - Memory Signals	6
Intel Springdale - AGP & LDT Signals	7
Intel ICH5 - PCI & IDE & AC97 Signals	8
Intel ICH5 - Other Signals	9
Clock - Cypress CY28405 & BIOS	10
DDR System Memory 1 , 2	11
SIO-W83627THF & KB/MS & FDD	12
COM,LPT	13
AGP SLOT & FAN CONTROL	14
PCI Slots 1 & 2 & 3	15
LAN RTL8110S/8100C	16
ALC655 / Connectors	17
USB CONNECTORS	18
IDE & SATA & Game port	19
ATX, FRONT PANEL	20
ACPI Controller MS7	21
VRM10 -INTERASIL 6556B	22
MEM,VCC_DAC & VTT Controller	23
VIA 6307/6306 1394	24
PULL HIGH RESISTORS & RTC	25
GPIO & JUMPER SETTING	26
POWER DELIVERY & MANUAL PART	27
REVISION HISTORY	28

Block Diagram

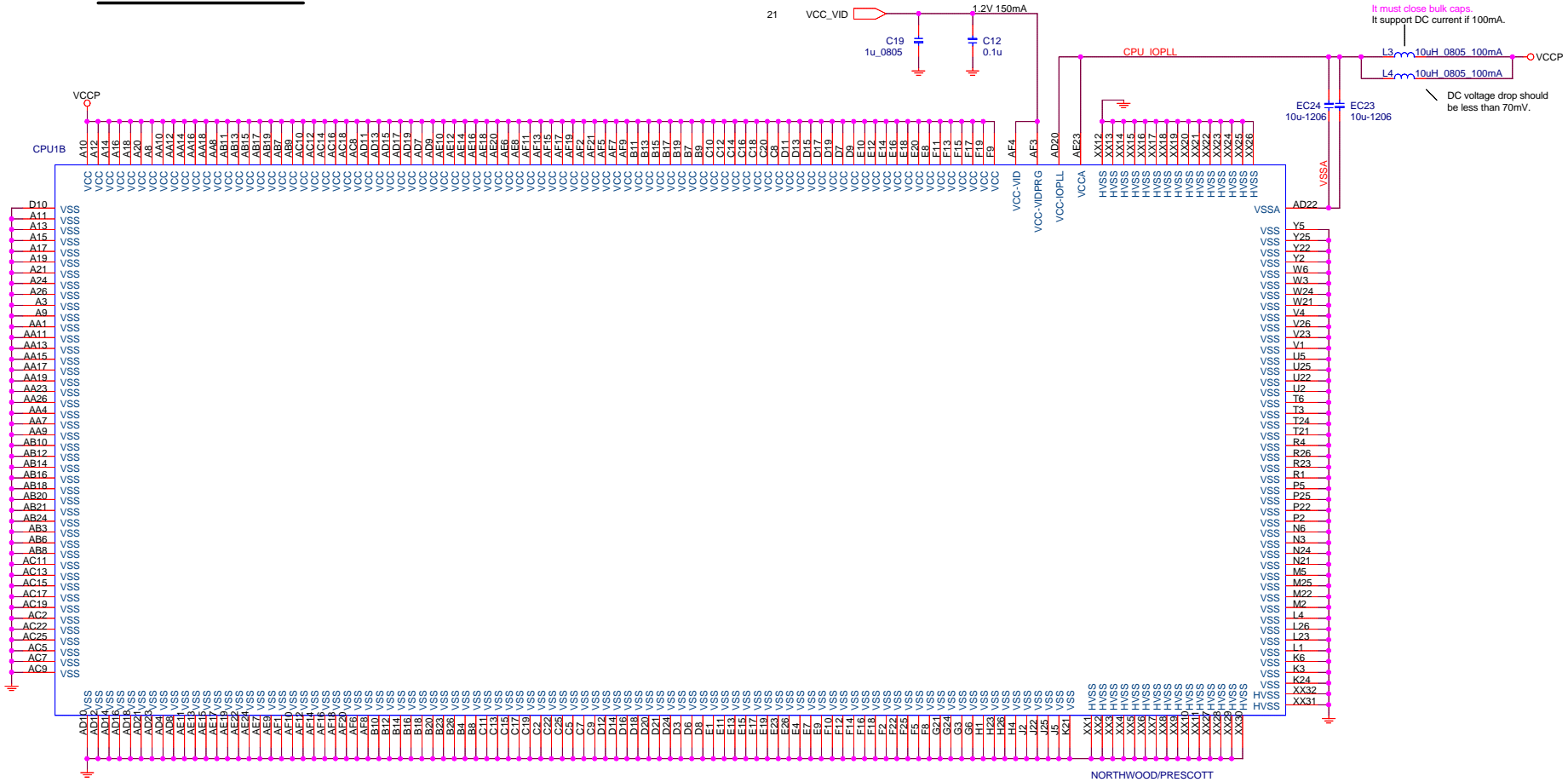


Micro-Star	Title	MS-7037	Rev	20A
	Document Number	BLOCK DIAGRAM		
Last Revision Date:		Thursday, May 06, 2004		
Sheet		2	of	31

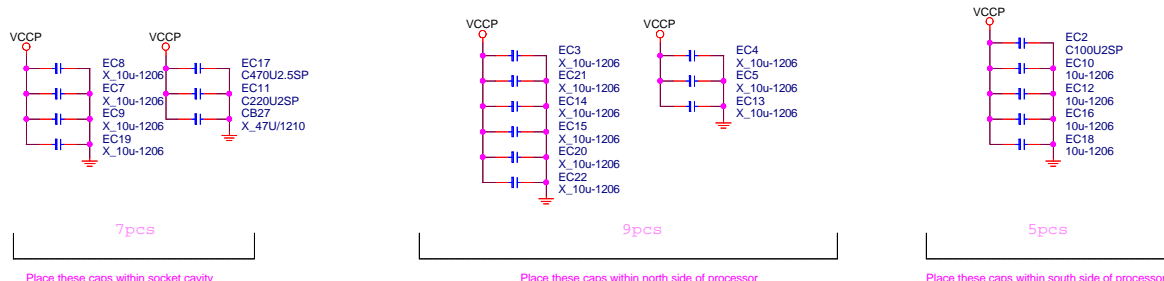


Micro-Star	Title MS-7037	Rev 20A
Document Number Intel mPGA478B - Signals		
Last Revision Date: Monday, May 24, 2004		Sheet 3 of 31

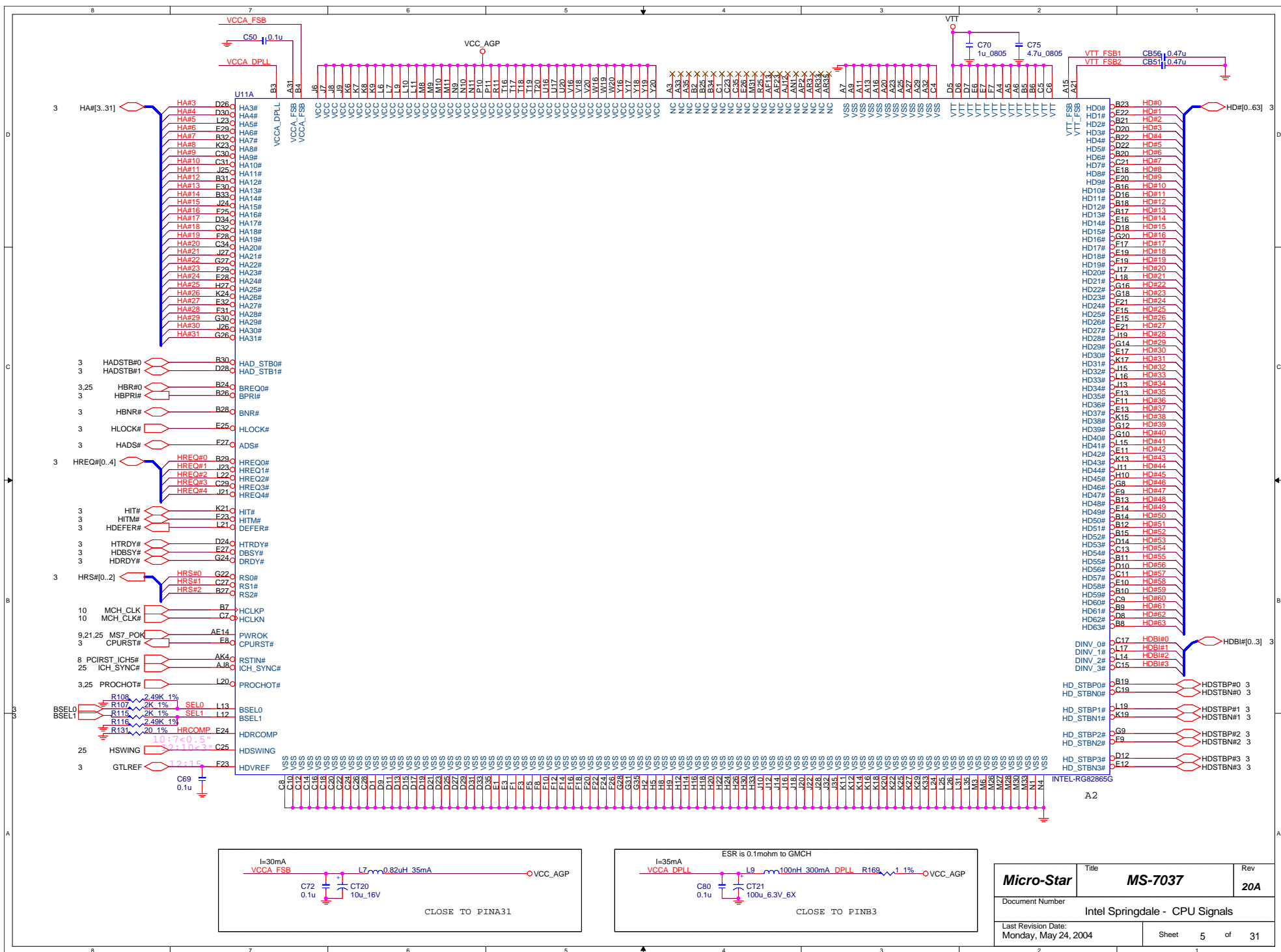
CPU VOLTAGE BLOCK



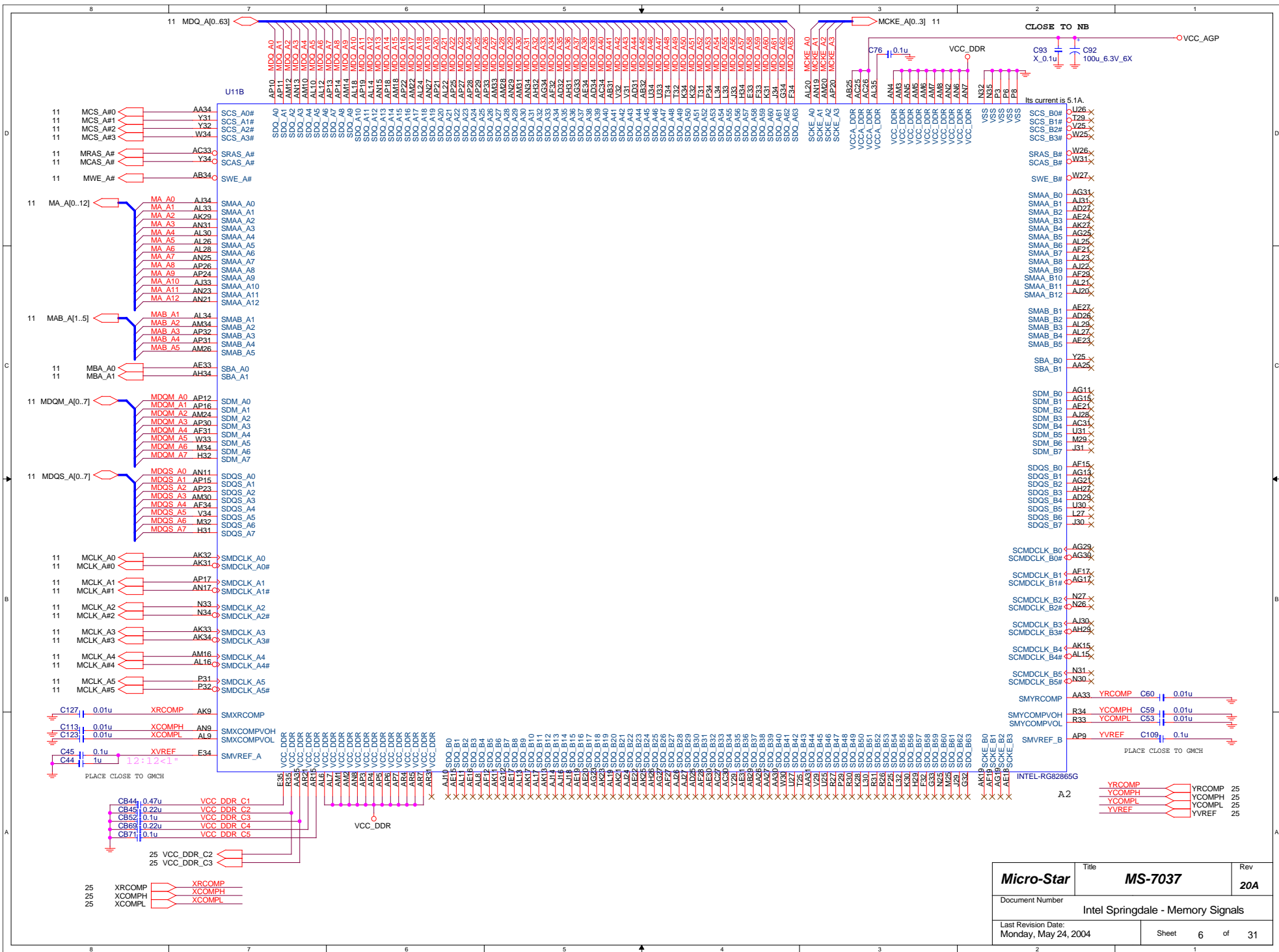
CPU DECOUPLING CAPACITORS



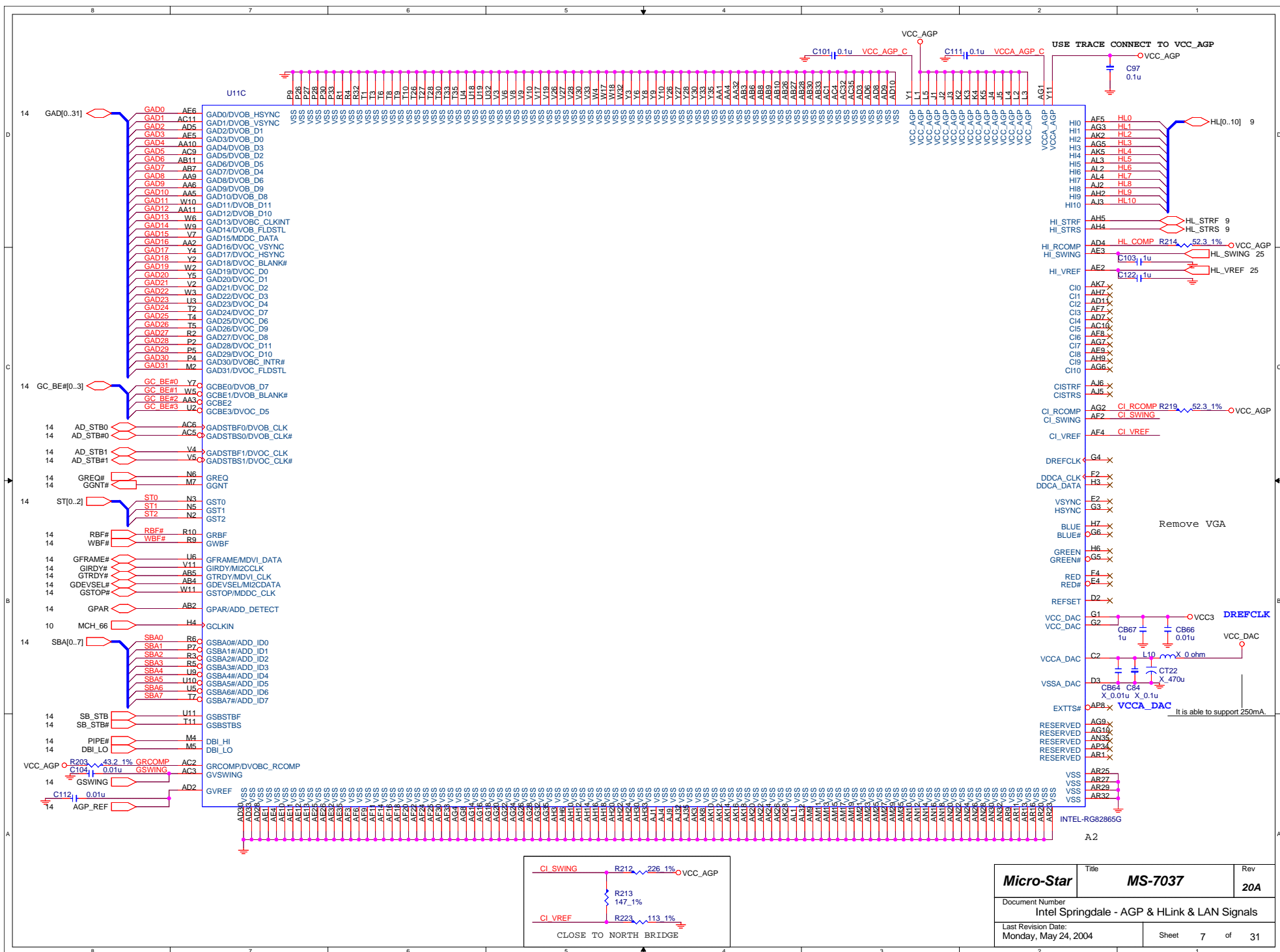
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	Document Number	Intel mPGA478B - Power		
	Last Revision Date:	Monday, May 24, 2004		
Sheet		4	of	31

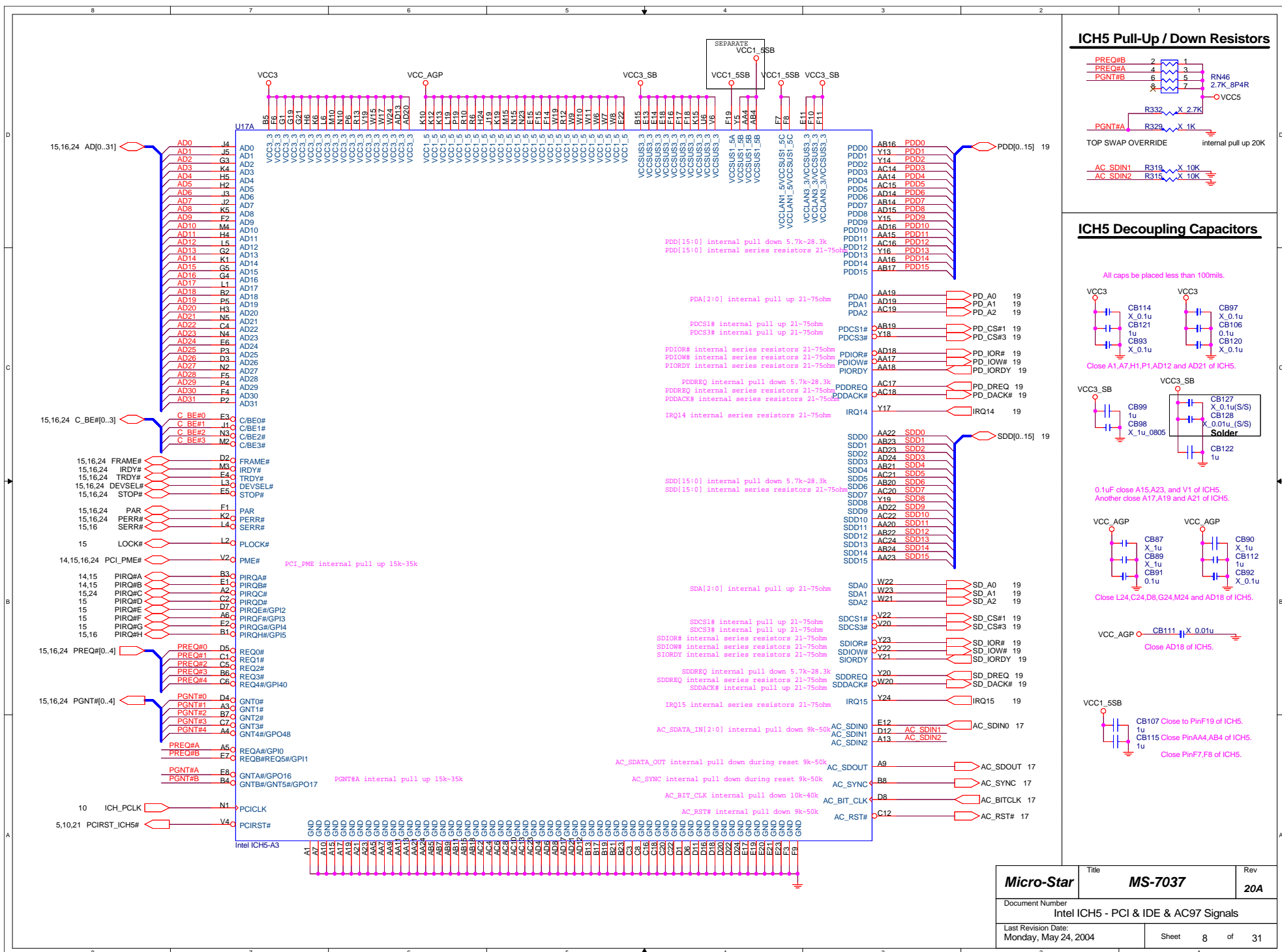


Micro-Star	Title	MS-7037	Rev	20A
Document Number	Intel Springdale - CPU Signals			
Last Revision Date:	Monday, May 24, 2004			Sheet 5 of 31

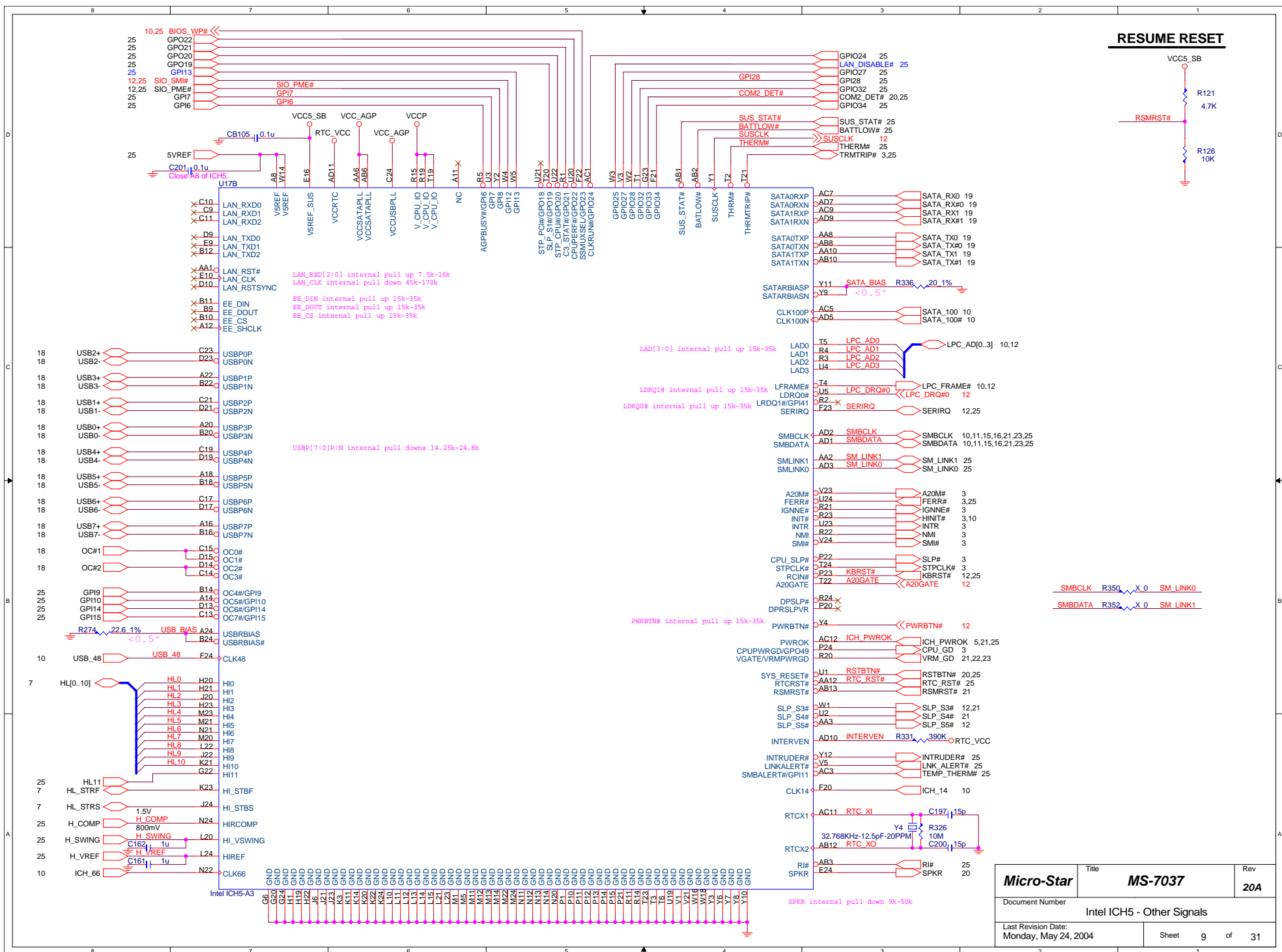


Micro-Star	Title	MS-7037	Rev	20A
	Document Number	Intel Springdale - Memory Signals		
Last Revision Date: Monday, May 24, 2004		Sheet	6	of 31

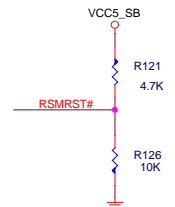




Micro-Star	Title	MS-7037	Rev	20A
Document Number				
Intel ICH5 - PCI & IDE & AC97 Signals				
Last Revision Date: Monday, May 24, 2004		Sheet 8 of 31		



RESUME RESET



Micro-Star	Title	MS-7037	Rev	20A
Document Number	Intel ICH5 - Other Signals			
Last Revision Date:	Monday, May 24, 2004			Sheet 9 of 31

DDR DIMM1

DDR DIMM2

DDR Terminational Resistors

SIGNALS

SIGNALS

POWER

POWER

DECOUPLING CAPACITORS

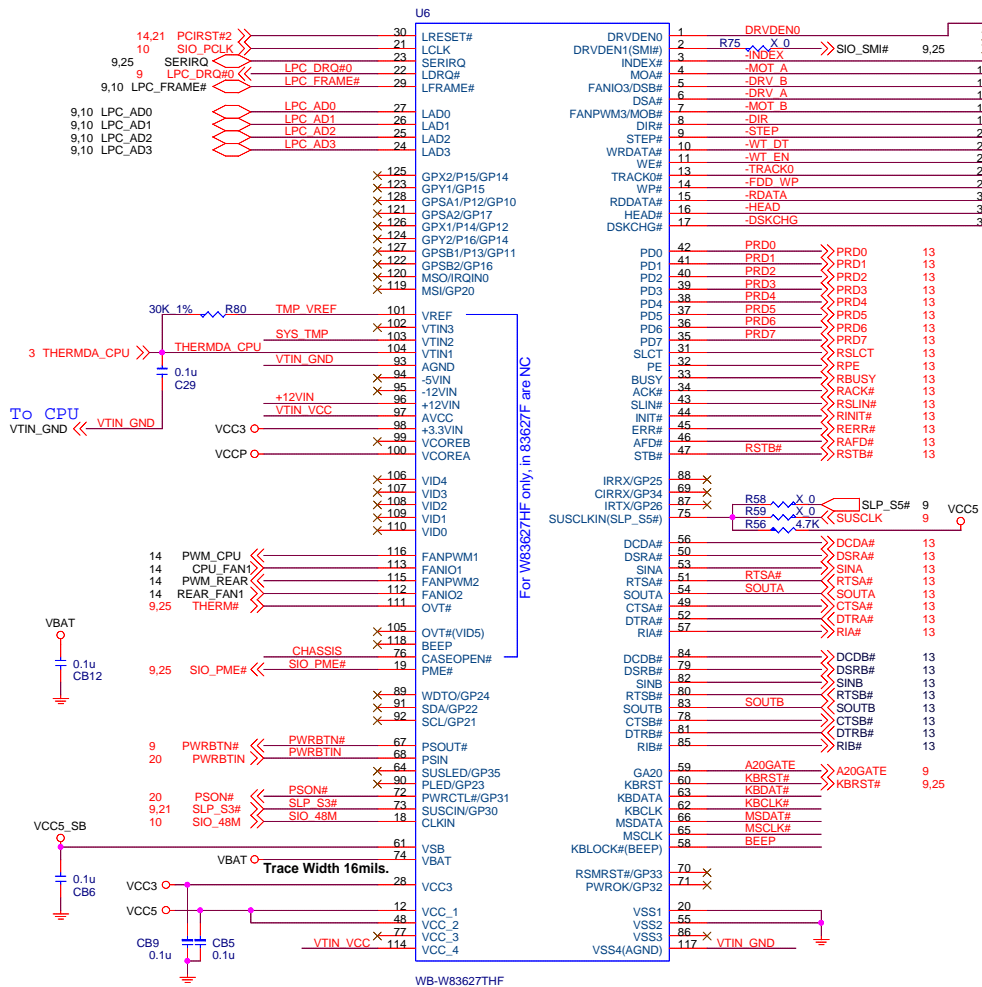
DECOUPLING CAPACITORS

ADDR.=1010000B(A0H)

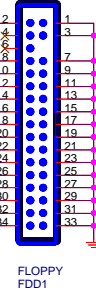
ADDR.=1010001B(A2H)

Micro-Star	Title	MS-7037	Rev	20A
Document Number	DDR DIMM 1 & 2			
Last Revision Date: Monday, May 24, 2004	Sheet	11	of	31

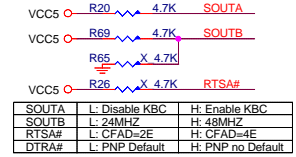
LPC SUPER I/O W83627THF



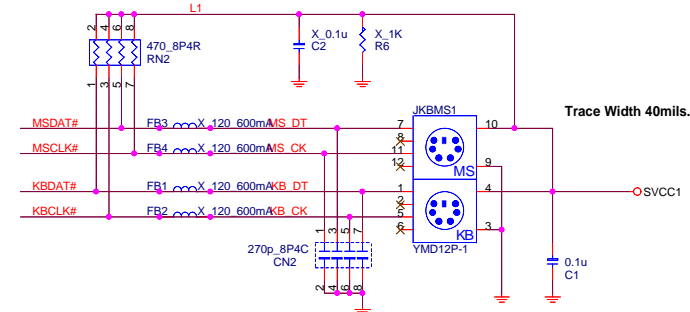
FLOPPY CONNECTOR



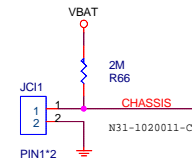
SUPER I/O STRAPPING RESISTOR



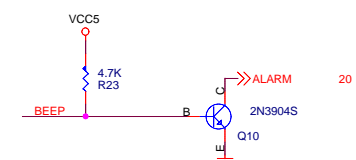
PS2 KEYBOARD & MOUSE CONNECTOR



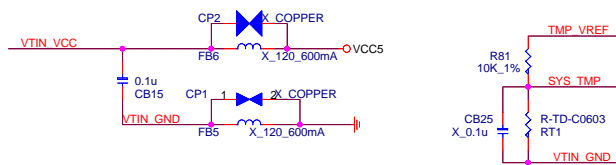
Chassis Intrusion



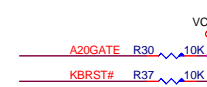
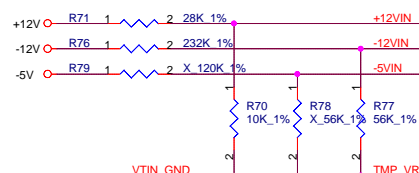
SPEAKER BLOCK



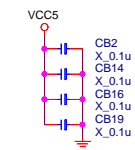
THERMAL RESISTOR BLOCK



NOTE: LOCATE CLOSE STATUS PANEL

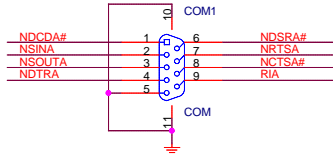
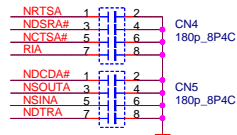
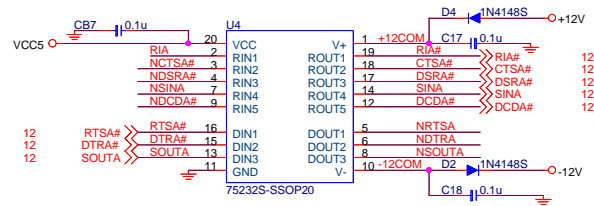


LPC I/O DECOUPLING CAPACITORS

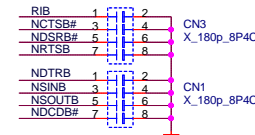
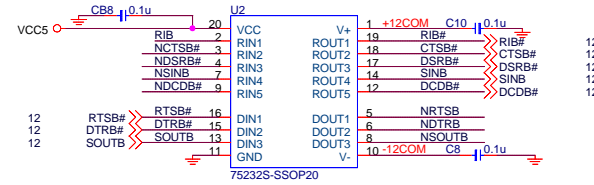


Micro-Star	Title	MS-7037	Rev	20A
Document Number	SIO-W83627HF & KB/MS & FDD			
Last Revision Date:	Monday, May 24, 2004			
Sheet	12	of	31	

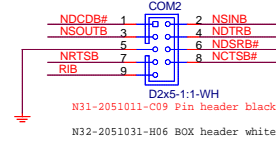
SERIAL PORT 1



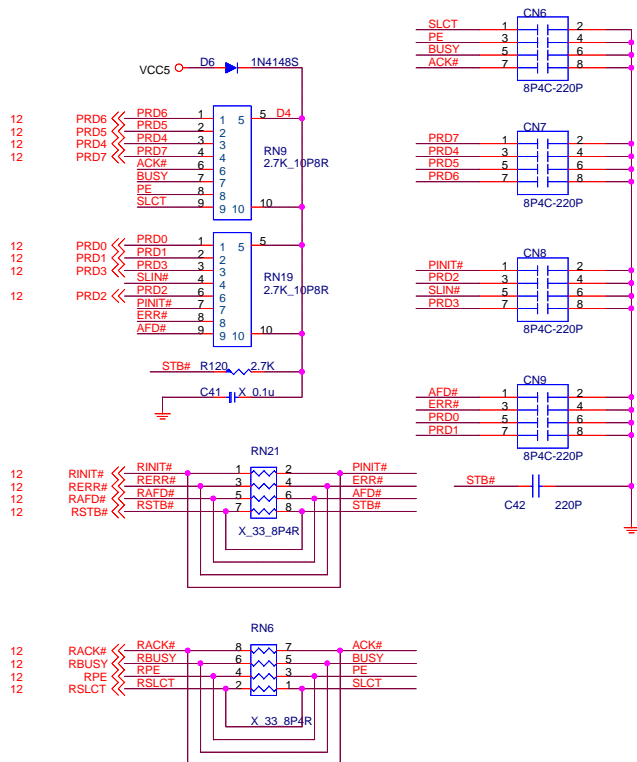
SERIAL PORT 2



COM2 HEADER



PARALLAL PORT



VCC5 = 60mils trace / 15 mils space

VCCq	8.0A
VCC3	6.0A
VCC12	1.0A
VCC5	2.0A
VCC3_SB	0.75A

CHECK PART NUMBER

AGP1

AGP2

Legend:

- Red box: Pin not present in this version
- Blue box: Pin not present in this version
- Green box: Pin not present in this version
- Yellow box: Pin not present in this version
- White box: Pin not present in this version

Pin-to-Pin Comparison Table:

AGP1 Pin	AGP1 Function	AGP2 Pin	AGP2 Function
B1	OVRCNT	A1	+12V
B2	5V	A2	G_DET#
B3	5V	A3	
B4	USB+	A4	
B5	GND	A5	
B6	INTB	A6	
B7	CLK	A7	
B8	-REQ	A8	
B9	3.3V	A9	VCC3
B10	ST0	A10	
B11	ST2	A11	
B12	-RBF	A12	
B13	RESERVED	A13	
B14	RESERVED	A14	
B15	SBA0	A15	
B16	3.3V	A16	
B17	SBA2	A17	
B18	SB_STB	A18	
B19	GND	A19	
B20	GND	A20	
B21	SBA6	A21	
B22	RSVD/KEY	A22	
B23	GND/KEY	A23	
B24	AUX3/KEY	A24	
B25	3.3V/KEY	A25	
B26	AD31	A26	
B27	AD29	A27	
B28	3.3V	A28	
B29	AD27	A29	
B30	AD25	A30	
B31	GND	A31	
B32	AD_STB1	A32	
B33	AD23	A33	
B34	VDDQ	A34	
B35	AD21	A35	
B36	AD19	A36	
B37	GND	A37	
B38	AD17	A38	
B39	C-BE2	A39	
B40	VDDQ	A40	
B41	-IRDY	A41	
B42	AUX3/KEY	A42	
B43	GND/KEY	A43	
B44	RSVD/KEY	A44	
B45	3.3V/KEY	A45	
B46	-DEVSEL	A46	
B47	VDDQ	A47	
B48	-PERR	A48	
B49	GND	A49	
B50	-SERR	A50	
B51	C-BE1	A51	
B52	VDDQ	A52	
B53	AD14	A53	
B54	AD12	A54	
B55	GND	A55	
B56	AD10	A56	
B57	AD8	A57	
B58	VDDQ	A58	
B59	AD_STB0	A59	
B60	AD7	A60	
B61	GND	A61	
B62	AD5	A62	
B63	AD3	A63	
B64	VDDQ	A64	
B65	AD1	A65	
B66	VREF CG	A66	

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PIRQ#A / PIRQ#B

VCC_AGP

+12V

VCC_AGP

GPERR#

AGPREF

AGP_REF 7

0B

Q45 2N3904S

Q46 2N3904S

Q47 2N7002S

R249 8.2K

R243 8.2K

R240 39.2 1%

R246 8.2K

R236 100

R234 39.2 1%

R235 100 1%

R247 300

R248 4.7K

R245 60.4 1%

C131 0.1u

C132 X.0.1u

G_DET#

DET# B

DET# E

DET# C

G_DET# :L(3.0) =GSWING:0.8V

G_DET# :H(2.0) =AGP_REF:0.75V

AGP_REF:0.35V

CHECK VALUE

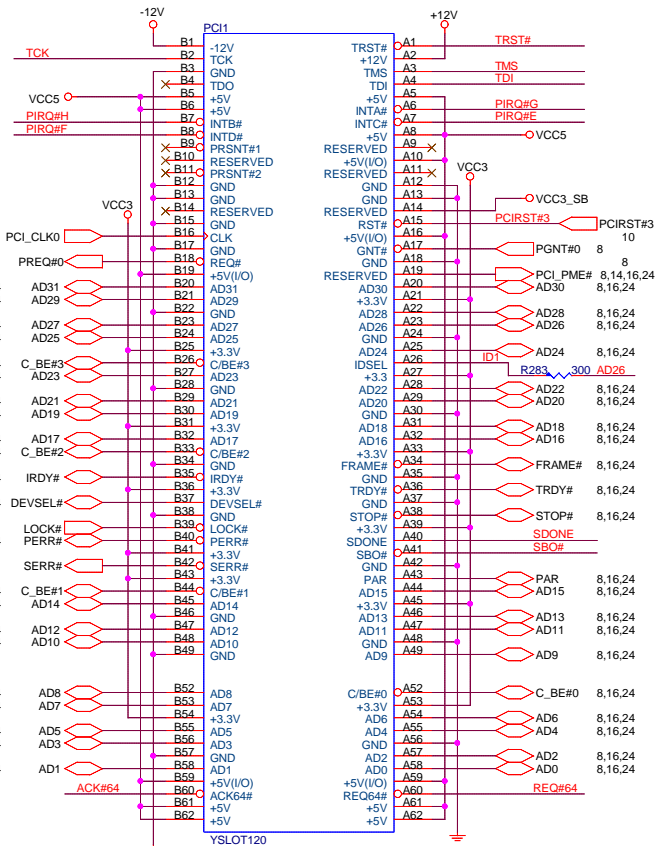
GSERR# R237 8.2K VCC_AGP

GSERR# R237 8.2K VCC_AGP

Three circuit diagrams illustrating different decoupling topologies for power supply rails:

- VCC3_SB:** A series combination of two capacitors, CB84 and CB83, both rated at 0.1uF, connected to ground.
- VCC3_AGP:** A more complex network starting with an inductor CT24 (1000uH) in series with a capacitor CB74 (0.1uF). This is followed by a parallel combination of capacitors CB86, CB85, and CB87, all rated at 0.1uF, connected to ground.
- VCC3:** A parallel combination of three capacitors, CB82, CB73, and CB77, all rated at 0.1uF, connected to ground.

Micro-Star	Title MS-7037	Rev 20A
Document Number		
AGP SLOT & FAN CONTROL		
Last Revision Date: Monday, May 24, 2004	Sheet 14 of 31	



FRAME# 2 1 VCC5
IRDY# 4 3
TRDY# 6 5 RN42
DEVSEL# 8 7 2.7K_8P4R

8 8.24
STOP# 2 1 VCC5
LOCK# 4 3
PERR# 6 5 RN45
SERR# 8 7 2.7K_8P4R

VCC5 CB110 X 0.1u VCC3
CB78 X 0.1u

PREQ#0 2 1 VCC5
PREQ#1 4 3
PREQ#2 6 5 RN49
PREQ#3 8 7 2.7K_8P4R

8 8.24
PREQ#4 R330 2.7K

REQ#64 R285 4.7K VCC5
ACK#64 R286 4.7K

TMS R364 X 4.7K
TDI R365 X 4.7K

TCK R345 X 4.7K
TRST# R346 X 4.7K

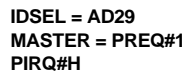
SDONE SMBCLK 9,10,11,16,21,23,25

SBO# SMBDATA 9,10,11,16,21,23,25

Part	Value
Micro-Star	MS-7037
Rev	

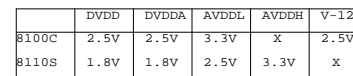
Micro-Star	Title	MS-7037	Rev	20A
Document Number				
PCI 1& 2 & 3 Slots				
Last Revision Date:		Monday, May 24, 2004	Sheet	15 of 31

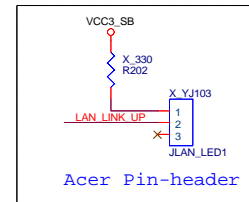
R287 2.49K for 8110S; 5.6k for 8100C



8,15,24 C_BE#[0..3]

8,15,24 AD[0..31]

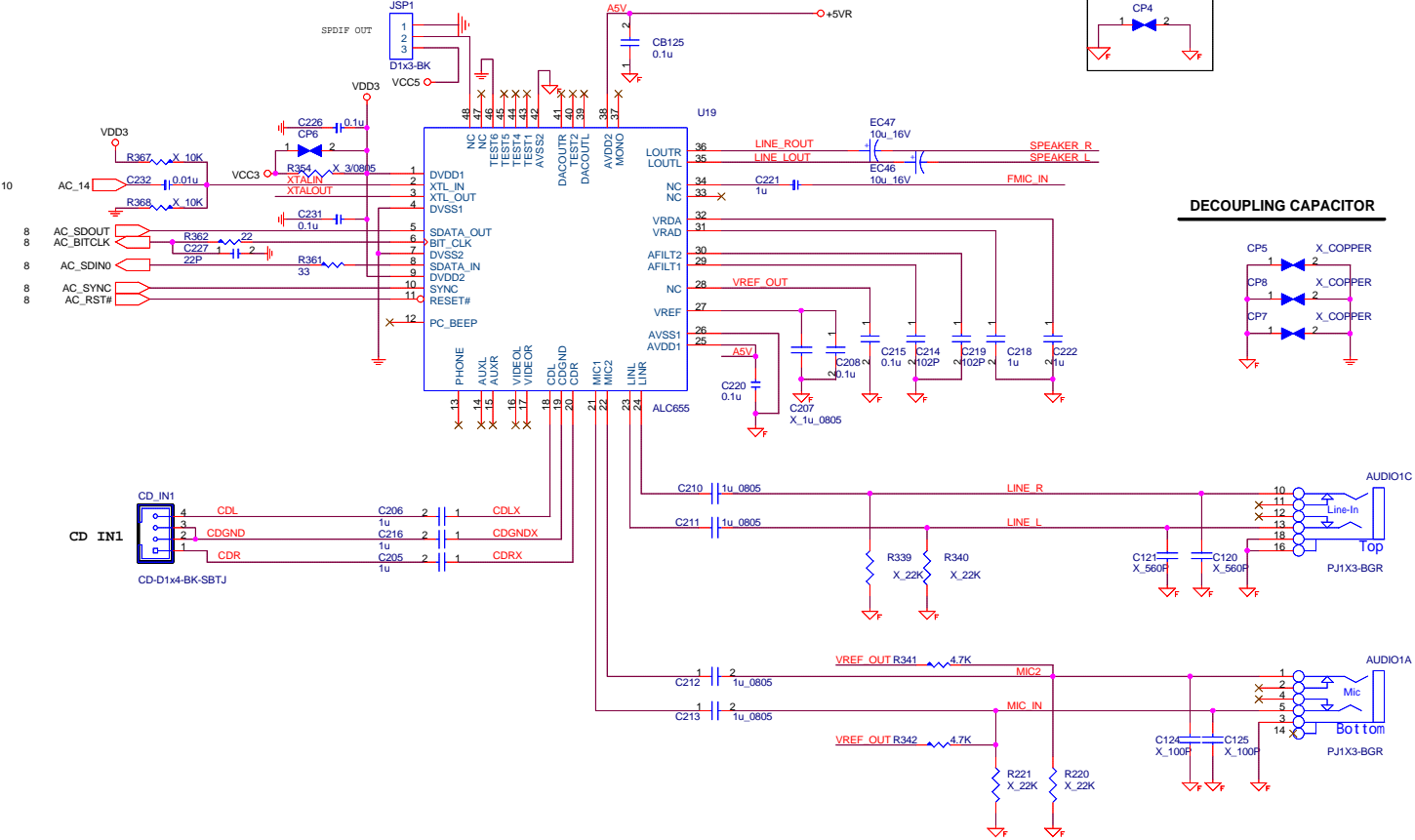




```
GbE: 8110S LAN(1000M)
TE: 8100C LAN(10/100M)
L: With LAN option
X: No Stuff
```

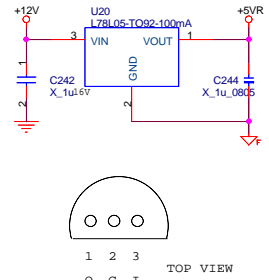
Micro-Star	Title	MS-7037	Rev	20A
Document Number				
LAN RTL8110S/8100C				
Last Revision Date: Monday, May 24, 2004		Sheet	16	of 31

ALC655 AC97 CODEC

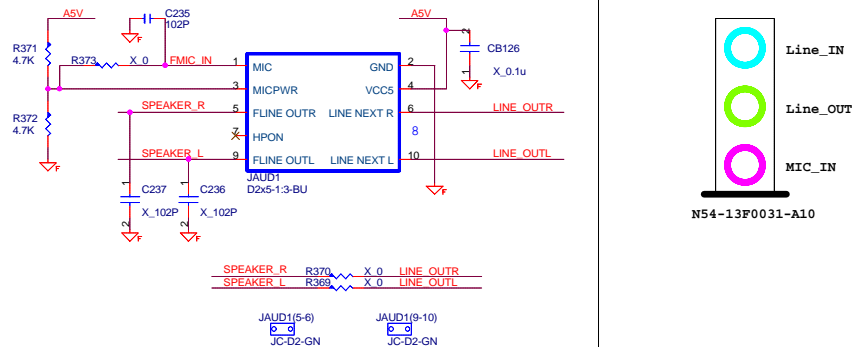


AUDIO CODE REGULATORS

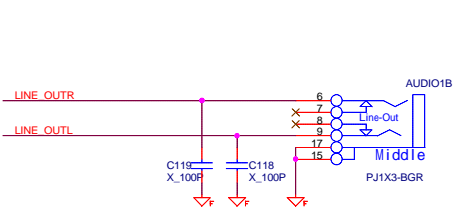
Trace Width 30mils.



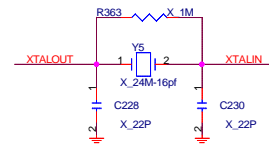
Intel Front Audio Connector



SPEAKER OUT JACK

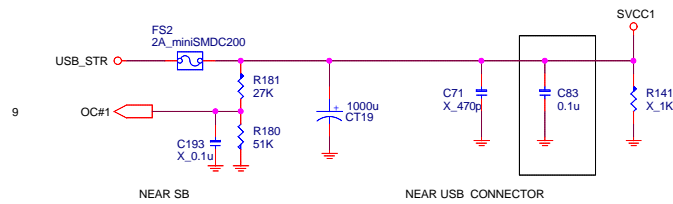


AUDIO CODE CRYSTAL CIRCUIT

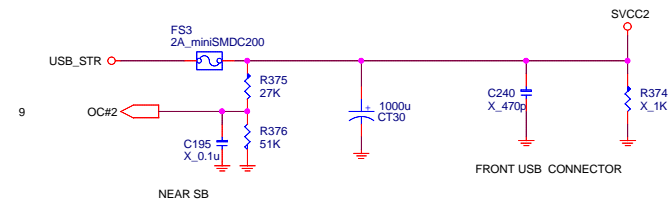


Micro-Star	Title	MS-7037	Rev	20A
	Document Number	ALC655		
Last Revision Date:		Monday, May 24, 2004	Sheet	17 of 31

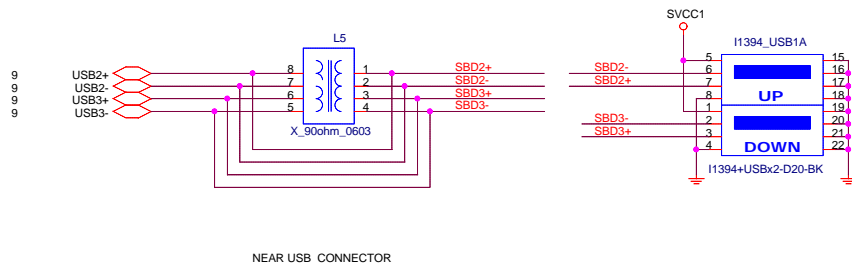
POWER CIRCUIT FOR USB PORT 0,1,2,3



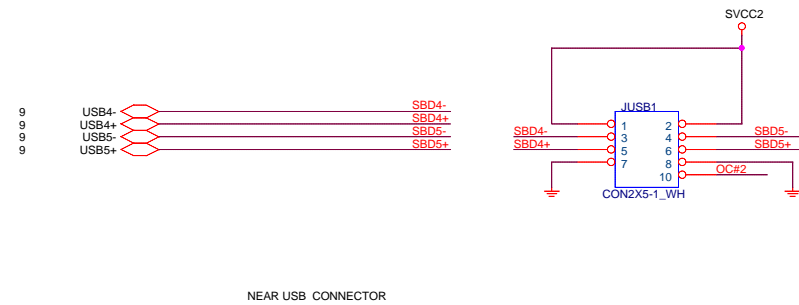
POWER CIRCUIT FOR USB PORT 4,5,6,7



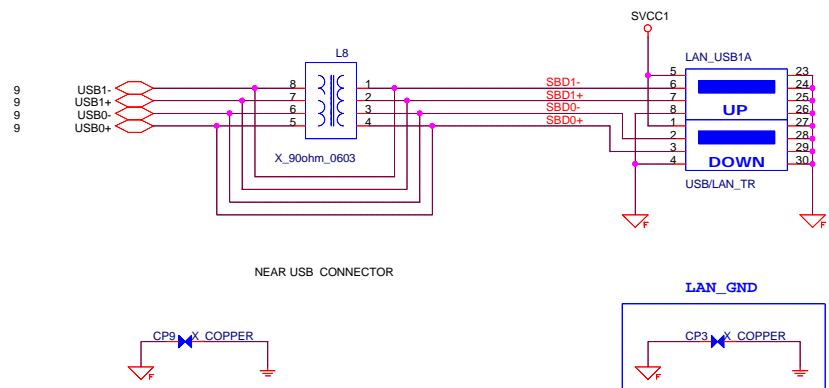
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



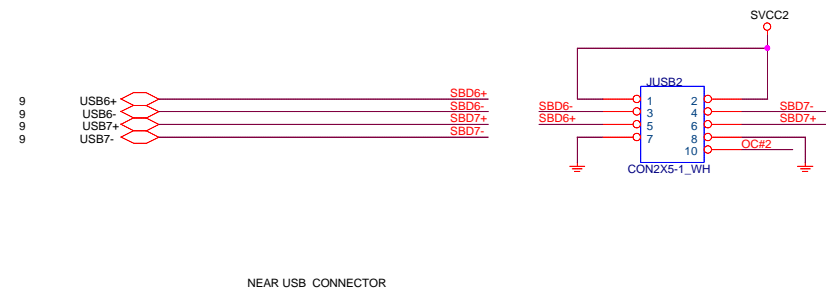
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



REAR PANEL USB CONNECTOR FOR USB PORT 2,3

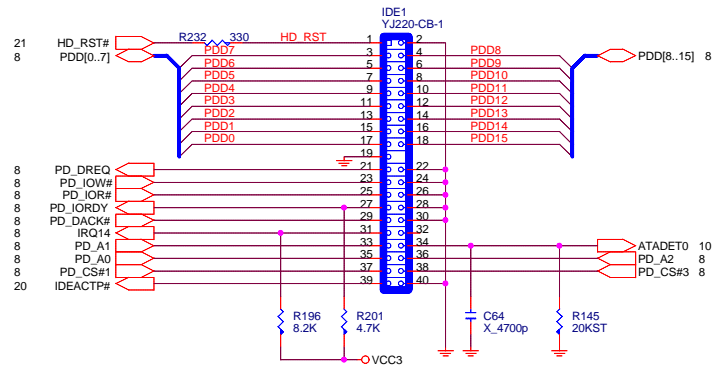


FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

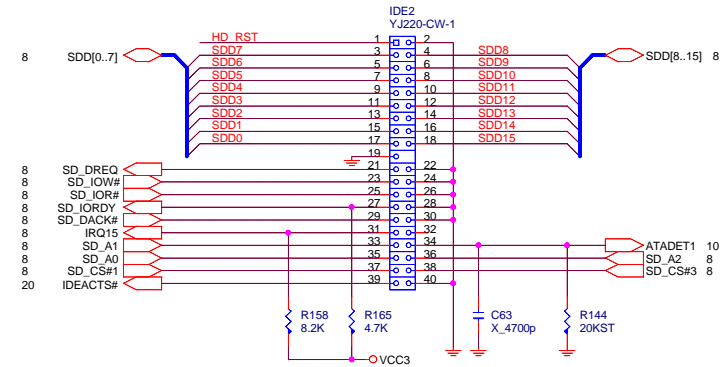


Micro-Star	Title	MS-7037	Rev	20A
	Document Number	USB Connectors		
Last Revision Date:		Monday, May 24, 2004	Sheet	18 of 31

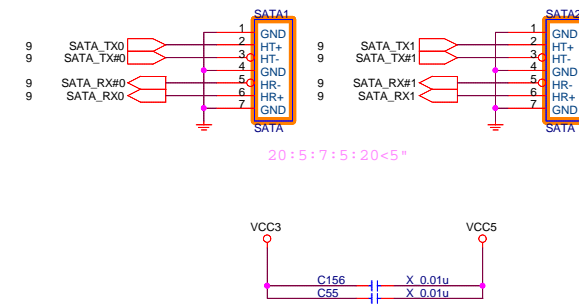
PRIMARY IDE BLOCK



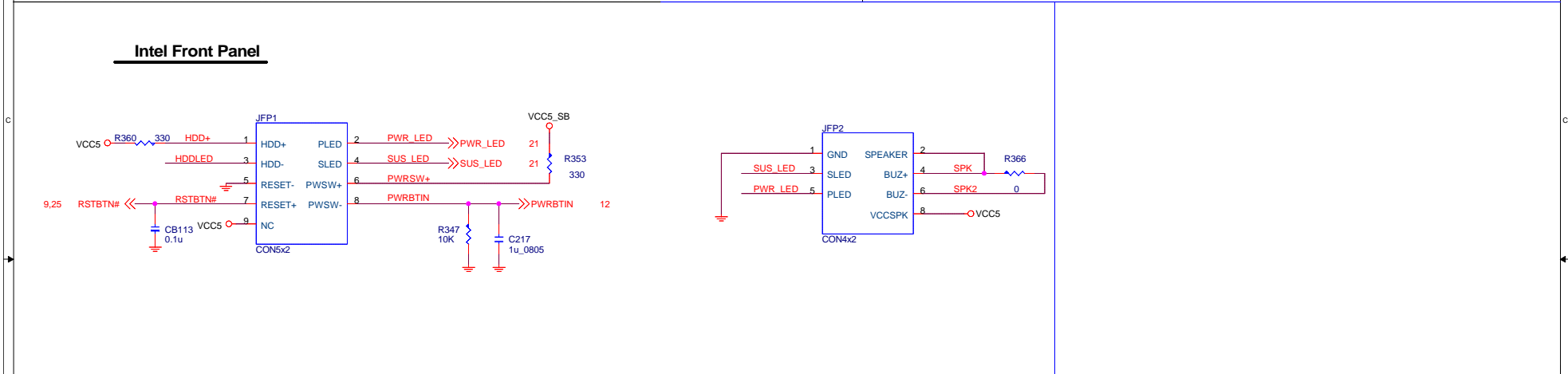
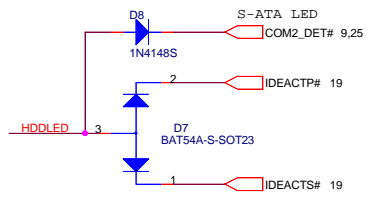
SECONDARY IDE BLOCK



SERIAL ATA CONNECTOR BLOCK



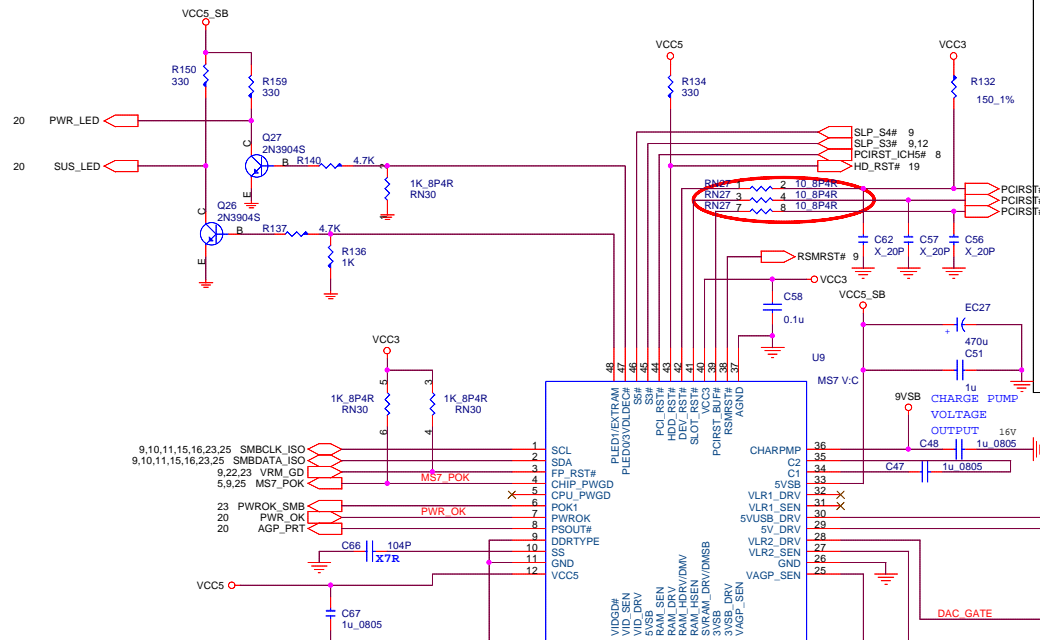
Micro-Star	Title	MS-7037	Rev	20A
	Document Number	IDE & SATA & Game port		
Last Revision Date:		Monday, May 24, 2004		
Sheet		19	of	31

[illegible][illegible]

ACPI Controller

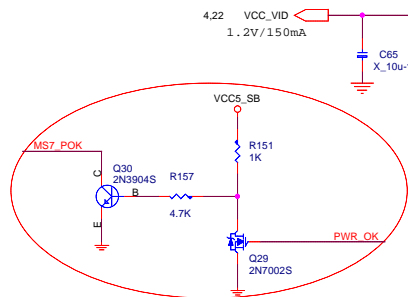
	ICH5 300mA
PCI	375+20+20= 415mA
<hr/>	
VCC3_SB	715mA

Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
MEM_STR	Main	Standby	0V



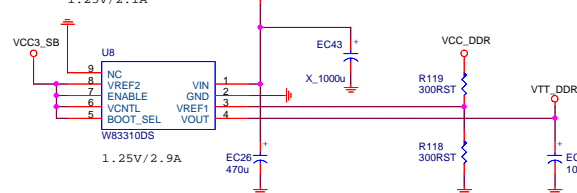
VCC_VID / VID_GOOD

Place MOSFET near CPU



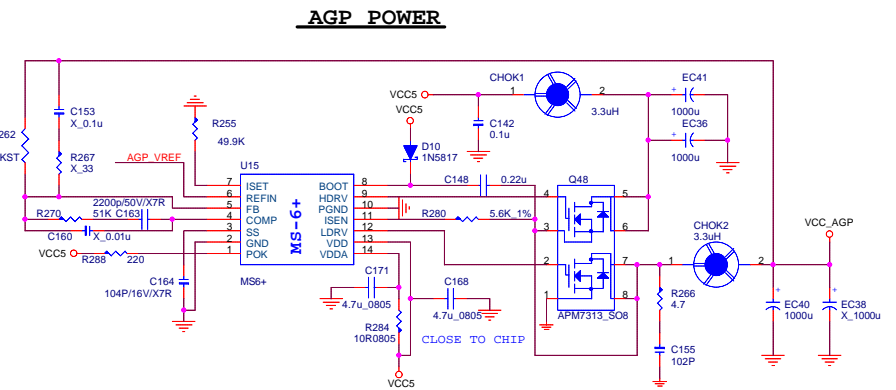
DDR VTT Power

1.25V/2.1A

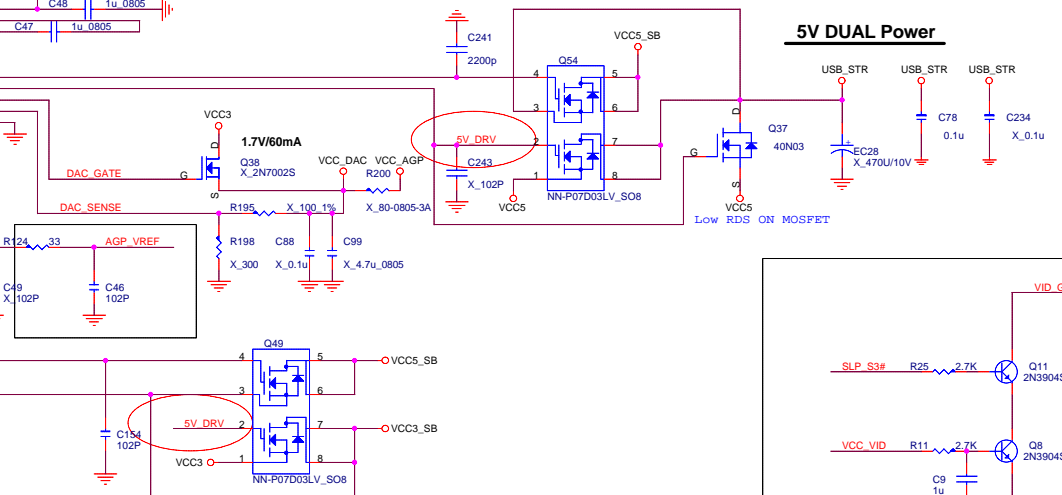


DDR 2.5V Power

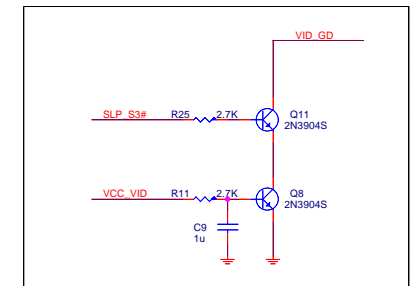
2.5V/7A(DIMM)+5A(NB)



$I_o \times R_{ds(on)} = I_{sen}(72\mu A) \times R_{sen}$
 $I_d = 6A, I_d(max) = 24A$
 $R_{ds(on)}/10V = 21m\ \Omega \sim 28m\ \Omega$
 $Overcurrent\ (4.7K\ \Omega) = 12A \sim 16A$

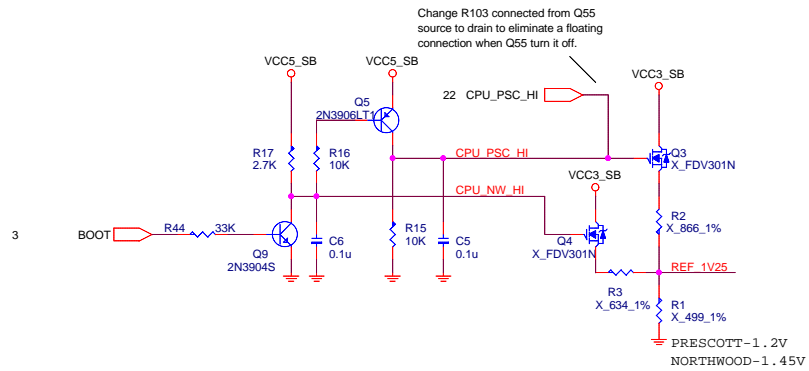


5V DUAL Power

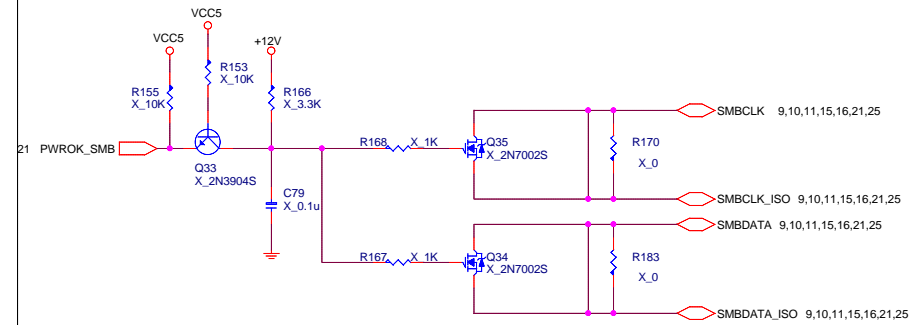
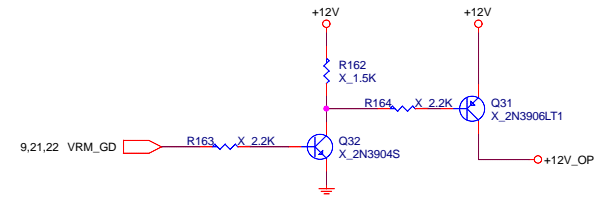


Micro-Star	Title MS-7037	Rev 20A
Document Number ACPI Controller MS7		
Last Revision Date: Monday, May 24, 2004		Sheet 21 of 31

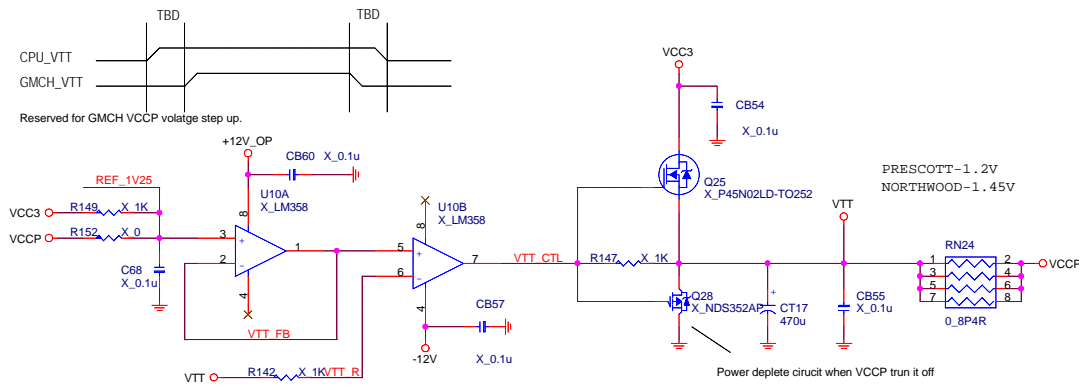
Intel reference GMCH VTT power cirucit



GMCH_VTT ON/OFF CIRCUIT



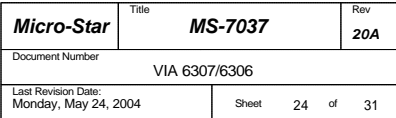
GMCH VTT Generator



Bootstrap pin are input rather then output on Intel Prescott processor, either it's internal weak pull-up but still need to identify it can be sufficient driving capability for out side ciruit. And the bootstrap pin power by core voltage so the outside circuit need to adjust the turn off voltage.

Micro-Star	Title	MS-7037	Rev	20A
Document Number	MEM,VCC_DAC & VTT Controller			
Last Revision Date:	Monday, May 24, 2004			
Sheet	23	of	31	

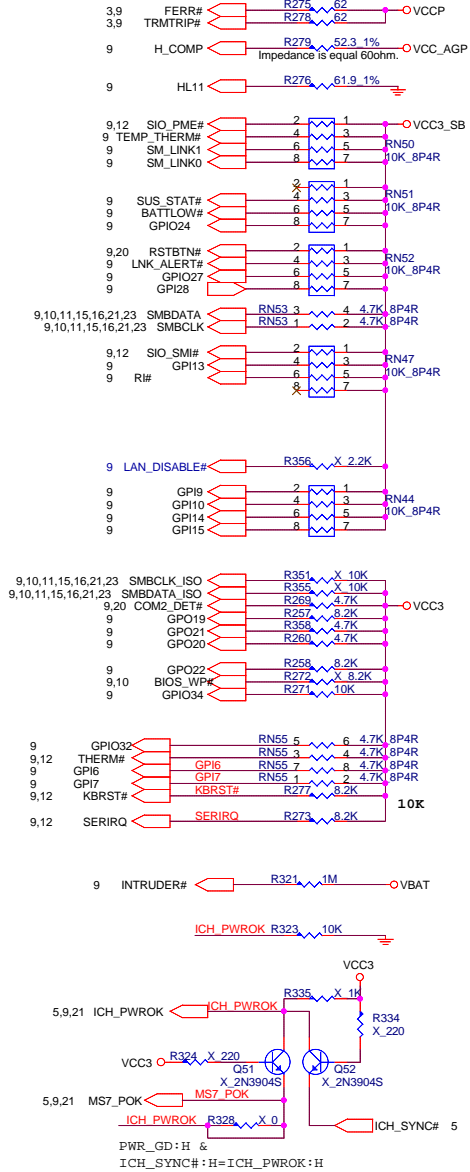
A



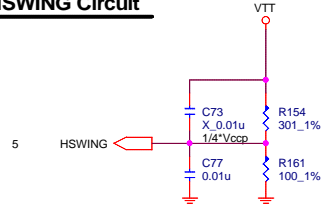
ICH5 STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO ICH5

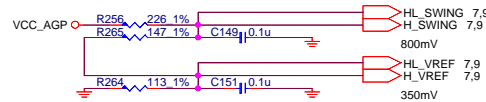
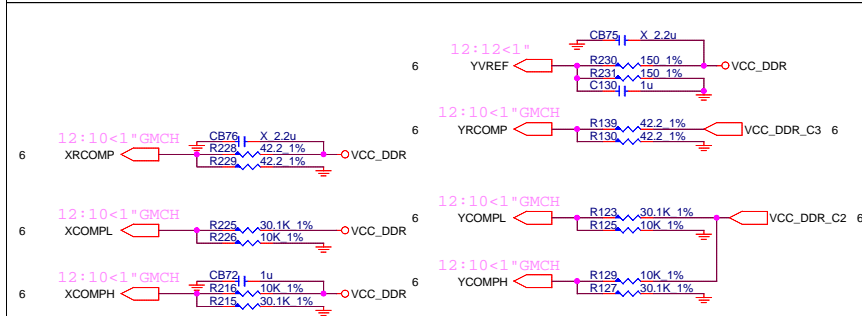
Trace length is less than 3inches to ICH5



HSWING Circuit

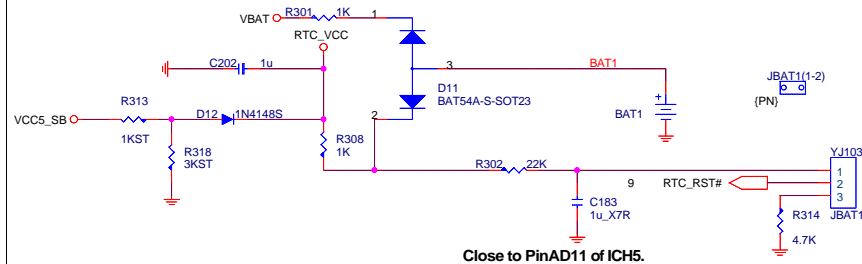


5VREF Sequencing Circuit



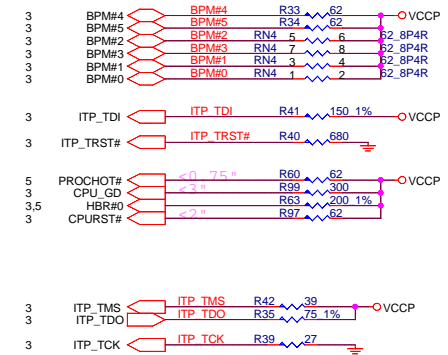
RTC BLOCK

CLR CMOS
1-2 Normal *
2-3 Clear CMOS



CPU STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO CPU



Micro-Star	Title MS-7037	Rev 20A
Document Number	PULL HIGH RESISTORS & RTC	
Last Revision Date: Monday, May 24, 2004	Sheet 25	of 31

ICH5

GPIO Pin	Type	Function	Power well
GPIO 0	I	PREQ#A	MAIN
GPIO 1	I	PREQ#B	MAIN
GPIO 2	I	PIRQ#E	MAIN
GPIO 3	I	PIRQ#F	MAIN
GPIO 4	I	PIRQ#G	MAIN
GPIO 5	I	PIRQ#H	MAIN
GPIO 6	I	GPI6	MAIN
GPIO 7	I	GPI7	MAIN
GPIO 8	I	SIO_PME#	RESUME
GPIO 9	I	OC4#	RESUME
GPIO 10	I	OC5#	RESUME
GPIO 11	I	TEMP_THERM#	RESUME
GPIO 12	I	SIO_SMI#	RESUME
GPIO 13	I	GPI13	RESUME
GPIO 14	I	OC#6	RESUME
GPIO 15	I	OC#7	RESUME
GPIO 16	O	PGNT#A	MAIN
GPIO 17	O	PGNT#B	MAIN
GPIO 18	O	GPO18	MAIN
GPIO 19	O	GPO19	MAIN
GPIO 20	O	GPO20	MAIN
GPIO 21	O	GPO21	MAIN
GPIO 22	OD	GPO22	MAIN
GPIO 23	O	BIOS_WP#	MAIN
GPIO 24	I/O	GPIO24	RESUME
GPIO 25	I/O	LAN_DISABLE#	RESUME
GPIO 27	I/O	GPIO27	RESUME
GPIO 28	I/O	GPIO28	RESUME
GPIO 32	I/O	GPIO32	MAIN
GPIO 33	I/O	COM2_DET#	MAIN
GPIO 34	I/O	GPIO34	MAIN
GPIO 40	I	PREQ#4	MAIN
GPIO 41	I	GPI41	MAIN
GPIO 48	O	PGNT#4	MAIN
GPIO 49	OD	CPU_GD	MAIN

default output
default output
default output
default output
default output
default output

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#G PIRQ#H PIRQ#E PIRQ#F	PCI_REQ#0 PCI_GNT#0	AD26	PCICLK0
PCI Slot 2	PIRQ#F PIRQ#G PIRQ#H PIRQ#E	PCI_REQ#4 PCI_GNT#4	AD25	PCICLK1
PCI Slot 3	PIRQ#E PIRQ#F PIRQ#G PIRQ#H	PCI_REQ#2 PCI_GNT#2	AD28	PCICLK2
LAN	PIRQH	PCI_REQ#1 PCI_GNT#1	AD29	LAN_PCLK
1394	PIRQC	PCI_REQ#3 PCI_GNT#3	AD23	1394_PCLK

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	AOH	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A4H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR
JAUD1	(5-6) (9-10) W/O FRONT AUDIO	WITH FRONT AUDIO

SIO

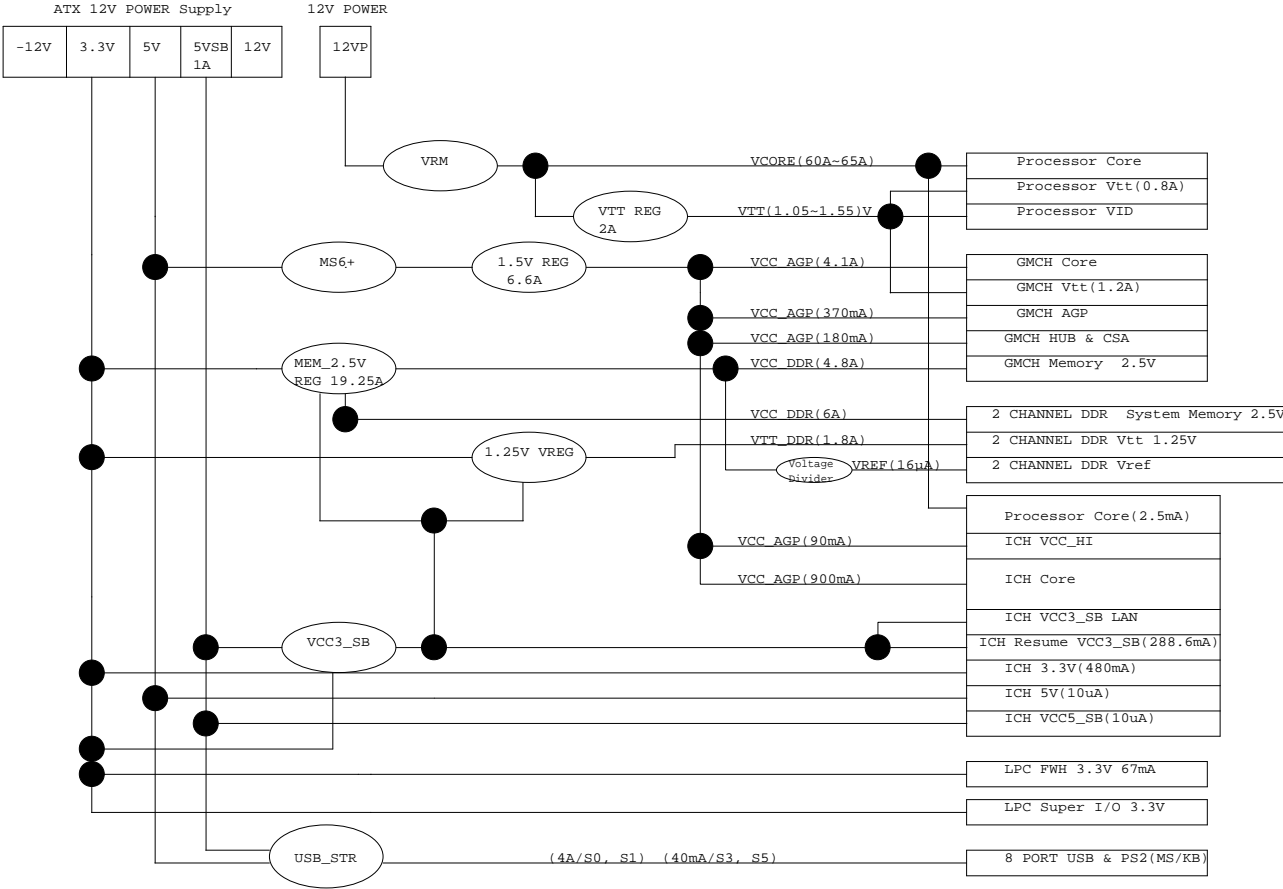
PIN NAME	USAGE	Input/Output	NOTES
GPIO10	UNUSED	INPUT	
GPIO11	UNUSED	INPUT	
GPIO12	UNUSED	INPUT	
GPIO13	UNUSED	INPUT	
GPIO14	UNUSED	OUTPUT	
GPIO15	VID5	INPUT	Low: VID add 0.0125V , High :by pass
GPIO16	UNUSED	OUTPUT	
GPIO17	UNUSED	OUTPUT	
GPIO20	UNUSED	OUTPUT	
GPIO21	SMBCLK_ISO	INPUT	SMBUS CLOCK
GPIO22	SMBDATA_ISO	INPUT / OUTPUT	SMBUS DATA
GPIO23	POWER_LED	OUTPUT	Default used MS-7
GPIO24	UNUSED	OUTPUT	
GPIO25	UNUSED	OUTPUT	IRRX
GPIO26	UNUSED	OUTPUT	
GPIO27	UNUSED	OUTPUT	
GPIO30	SLP_S3#	INPUT	S3 state indicator signal
GPIO31	PS_ON#	OUTPUT	Connector to Power Supply to turn on Power.
GPIO32	UNUSED	OUTPUT	
GPIO33	UNUSED	OUTPUT	
GPIO34	UNUSED	OUTPUT	
GPIO35	UNUSED	OUTPUT	

PCI RESET DEVICE

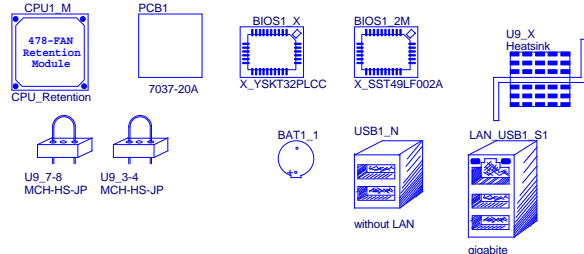
Signals	Target
PCIRST#1	LAN,1394
PCIRST#2	Super I/O,AGP slot
PCIRST#3	PCI1~3
PCIRST_ICH5#	Northbridge , FWH
HDDRST#	Primary, Scoundary IDE

Micro-Star	Title MS-7037	Rev 20A
Document Number GPIO & JUMPER SETTING		
Last Revision Date: Thursday, May 06, 2004		Sheet 26 of 31

POWER DELIVERY MAP



7037 PART



Micro-Star	Title	MS-7037	Rev	20A
	Document Number	POWER DELIVERY MAP & MANUAL PART		
	Last Revision Date:	Monday, May 24, 2004	Sheet	27 of 31

Revision History (Changes from Rev 100)

Sheet	Description
11,12	Change NB from 865G to 848P and support single channel 2 DDR
24	Change PWM to Intersil 6556B

Revision History (Changes from Rev 200)

Sheet	Description
10	Reserve FB9 for clock power
	Change R172 pin2 net VID_GD# to VID_GD